



SRI VENKATESWARA COLLEGE OF ENGINEERING
(AUTONOMOUS)

Karakambadi Road, Tirupati-517507

R20

EXAMINATION BRANCH

M.Tech I Semester (R20) Supplementary Examinations Feb-2026
TIME TABLE

Exam Timings: **10.00 AM TO 1.00 PM**

Date/Day	VLSI Design (VLSI D)	Computer Science and Engineering (CSE)
02-02-2026 (Monday)	CMOS Analog IC Design EC20DPC101	Mathematical Foundations of Computer Science CS20DPC101
04-02-2026 (Wednesday)	CMOS Digital IC Design EC20DPC102	Advanced Data Structures CS20DPC102
06-02-2026 (Friday)	Nanomaterials & Nanotechnology EC20DPE104	Machine Learning CS20DPE103
09-02-2026 (Monday)	CPLD and FPGA Architectures and Applications EC20DPE107	Data Science CS20DPE106
11-02-2026 (Wednesday)	Research Methodology and IPR EC20DPC109	Research Methodology and IPR CS20DPC109

Y. A. Suresh
Controller of Examinations
Date: 20-01-2026

Srinivas
Principal